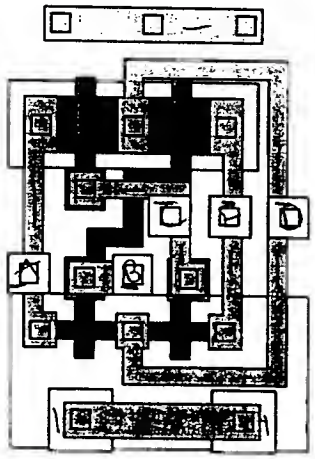
2000 midterm

QUESTION #1

MARKS: 15 (10 + 5)

Consider the following plot of a CMOS3DLM circuit.



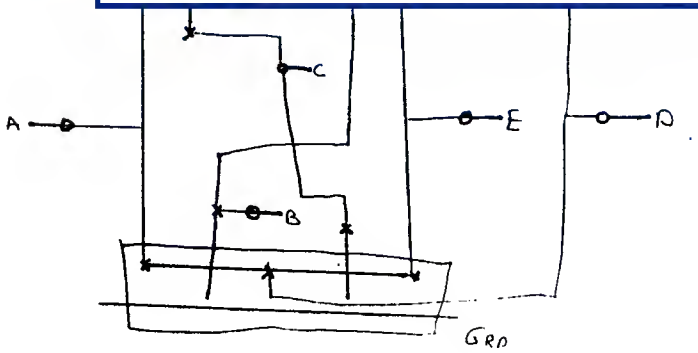
a) Determine the function of the circuit. Do this by drawing a STICKS diagram of the circuit and determining a truth table for the circuit. Use the following page. When drawing the STICKS diagram use standard E.E. 451.3 colors:

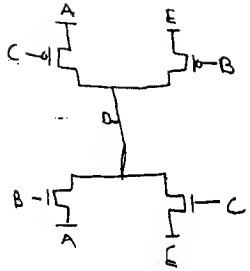
CMOS3DLM Layer	Color
N+ diffusion	Green
P+ diffusion	Orange
Polysilicon	Red
P-Well	Brown
Metal 1	Blue
Metal 2	Black
Contact Cut	X
Via	O

b) Indicate the number of each of the following:

- N channel transistors 2
- P channel transistors 2
- Input ports 3
- Output ports 2
- N-Well substrate contacts 0 3

4





10/

B	C	D	A	E
0	0	0	0	0
0	0	1	1	1
0	1	0	X	0
1	0	0	0	X
1	0	1	1	X
1	1	0	0	0
1	1	1	1	1
1	1	1	X	1

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"Well, I've wrestled with reality for 35 years, Doctor, and I'm happy to state I finally won out over it."

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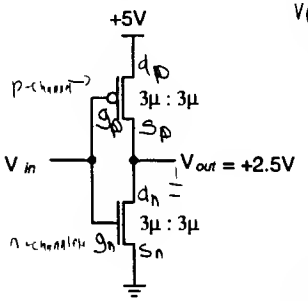
QUESTION #2

MARKS: 15 (15)

a) The following circuit is one of many standard designs for a CMOS inverter. Calculate the output voltage, V_{in}, when V_{out} is +2.5V. Important parameters are shown on Page 2. Show your calculation. Sizes shown are W:L.



p-CH $V_t = 0.8$ n-Chal $V_t = 0.7$

assume I_{ds} is equal for both transistors i.e no current flows through Vout

$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$

$\frac{\beta_n}{2}(V_{gs_n} - V_{t_n})^2 = \frac{\beta_p}{2}(V_{gs_p} - V_{t_p})^2$

$\frac{\beta_n}{2}[V_{in} - V_{tn}]^2 - \frac{\beta_p}{2}[5 - V_{in} - V_{tn}]^2$

$\beta_n = 5.35E\text{-}5$

$\beta_p = 0.000017257 \times 3 = 5.18E\text{-}5$

solve $V_{in} = 0.504 \times 3 = 1.512$

$V_{in} = 0.35V$

$V_{in} = V_{gsp} = V_{gsn}$

$\frac{\beta_n}{2}(V_{gsn}^2 - 2V_{tn}V_{gsn} + V_{tn}^2) = \frac{\beta_p}{2}(V_{gsp}^2 - 2V_{gsp}V_{tp} + V_{tn}^2)$

$0 = \beta_n V_{gsn}^2 - 2\beta_n V_{tn} V_{gsn} + \beta_n V_{tn}^2 + \beta_p(V_{gsn}+2.5)^2 - 2\beta_p V_{tp}(V_{gsn}+2.5) + \beta_p V_{tn}^2$

$= \beta_p V_{gsn}^2 + 5\beta_p V_{gsn} + 6.25\beta_p - 2\beta_p V_{tp} V_{gsn} - 5\beta_p V_{tp} + \beta_p V_{tn}^2$

$(\beta_n + \beta_p)V_{gsn}^2 + (-2\beta_n V_{tn} + 5 - 2\beta_p V_{tp})V_{gsn} + (\beta_n V_{tn}^2 + 6.25\beta_p + 5\beta_p V_{tp} + \beta_p V_{tn}^2)$

$= 0.001053 V_{gsn}^2 + (-0.00015778 + 0.00000596)V_{gsn} + (0.000168)$

$V_{gsn} = V_{in} = 1.46$ Volts (LOW)

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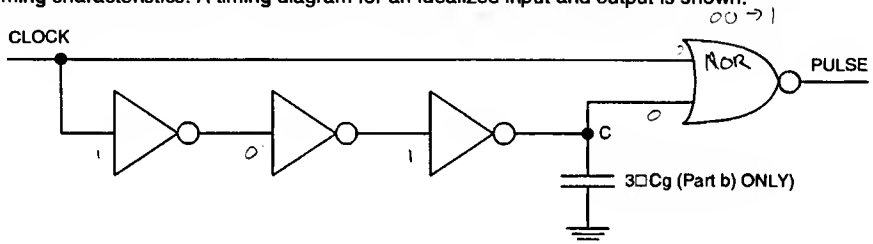
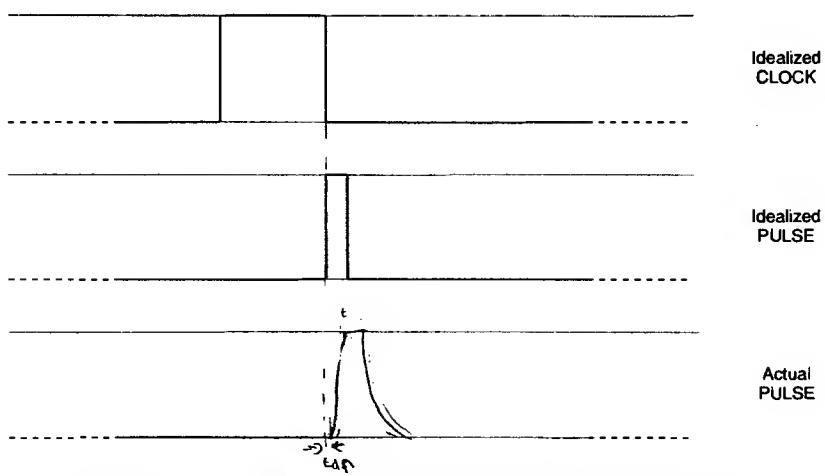
QUESTION #3

MARKS: 15 (10 + 5)

All parts of this question concern a negative-edge differentiator circuit (shown below). The operation of the circuit is such that when the CLOCK input goes to a logic 0, the circuit output (PULSE) pulses to a logic 1. The actual pulse characteristics such as delay, size, etc. depend on the gate timing characteristics. A timing diagram for an idealized input and output is shown.





a) Estimate, using appropriate equations, the output pulse characteristics of the circuit, taking into account device delays. Sketch the resulting waveform in the space provided (Actual PULSE). Assume that the duration of the CLOCK input signal at logic 0 is such that it is longer than any accumulated device delays (i.e., it does not go to logic 1 until the output PULSE has been generated). State any other assumptions that you make. Note that for this portion of the question there is no capacitor connected at point C.

b) What effect, if any, would occur if a 3□Cg capacitor is connected between point C and Vss (as shown on the diagram). Use an examination booklet for your answer. **Exact numerical results are not expected for this part of the question.**

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Question #3 Work Sheet

(a)

$t_{dr} = \frac{t_r}{3}$ $t_{df} = t_f/2$

$t_r = A_n C_L$ $t_f = A_p C_L$

using table 4.9 → Nand3 Spice & only #'s I could find

$t_{dr} = 0.255ns$

$t_{df} = 0.42ns$

$t_r = 0.45ns$

$t_f = 0.225ns$

pulse length = $2(0.42ns) + 2(0.255ns) + 2(0.42ns) + 0.42ns$

$= 2.61$ ns

$t_f = 2(0.42) = 0.84ns$

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(b) $3C_g = 3(6.9E\text{-}4pF)(L*W)$

→ would ensure better charge sharing
→ decrease rise and fall times
→ if big enough would eliminate spike

5

"In college I usually stayed up very late working with my roommates, Rob Stavis, Bob Stem, and Ken Stover, on important academic projects such as ordering pizza or assembling the legendary Two-Man Submarine. This was a miniature submarine that we obtained by sending $9.95 away to a company that advertised in Marvel comics. It came in a small, lightweight, very flat box, but when we assembled all the parts, we had an actual working two-man submarine in every possible respect except that (1) the two men could not be in it simultaneously, and (2) being constructed entirely out of cardboard, it was not ideally suited for the underwater environment."

SPECIFIC INSTRUCTIONS FOR THE EXAMINATION

1) All designs use standard CMOS3DLM design rules and layers. V_{DD} = +5V and V_{SS} = 0V.

2) Unless otherwise specified, normal substrate connections are assumed for all P-channel and N-channel transistors, i.e., V_{SS} for N-channel and V_{DD} for P-channel.

3) CMOS3DLM resistance and capacitance parameters are as follows:

Layer	Resistance	Capacitance
N-Diffusion	25.0 Ω/□	4.4E-4 pf/μm²
P-Diffusion	80.0 Ω/□	1.5E-4 pf/μm²
Polysilicon	18.0 Ω/□	6.0E-5 pf/μm²
Metal 1	0.035 Ω/□	2.7E-5 pf/μm²
Metal 2	0.030 Ω/□	1.4E-5 pf/μm²
N-Transistor	4275 Ω/□	See below
P-Transistor	13600 Ω/□	See below
Gate-channel	See above	6.9E-4 pf/μm²

4) Supplementary physical constants are as follows:

Constant	Symbol	Value	Units
Electron charge	q	1.602E-19	coulomb
Boltzmann's constant	k	1.38E-23	Joule/°K
Intrinsic carrier concentration of Si @ T=300°K (27°C)	n_i^2	2.1E+20	(carriers/cm³)²
Permittivity of free space	ε_0	8.854E-14	Farad/cm
Permittivity of Si	ε_{Si}	$11.7\varepsilon_0$	Farad/cm
Permittivity of SiO_2	ε_{ox}	$3.9\varepsilon_0$	Farad/cm

5) (H)SPICE process parameters are as follows:

Parameter	Name	N-channel	P-channel	Units
V_t	Zero-bias threshold voltage	0.7	0.8	Volts
K'	Process gain factor	40.0E-6	12.0E-6	A/V²
γ	Bulk threshold body factor	1.1	0.6	V$^{1/2}$
$2\lvert\phi_F\rvert$	Surface potential	0.6	0.6	V
λ	Channel length modulation factor	1.0E-2	3.0E-2	1/V
t_{ox}	Oxide thickness	5.0E-6	5.0E-6	cm
N_A or N_D	Substrate doping density	1.7E+16	5.0E+15	1/cm³
μ	Carrier surface mobility	775	250	cm²/(V·sec)

absolute

Name: [redacted] Student Number: [redacted]